CLAIMS

1. A delay locked loop control for a delay locked loop associated with a device responding to a system clock, the delay locked loop control comprising:

a device inactive decoder providing a device inactive signal when the delay locked loop need not continue adjusting a delay interval to synchronize with the system clock;

a stabilization detection device providing a stabilization signal when the device is stable after reacting to a command applied to the device; and

a delay lock coupled to the device inactive decoder and the stabilization detection device for locking the delay interval on receiving both the device inactive signal and the stabilization detection signal.

2. The delay locked loop control of claim 1 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a self-refresh command.

3. The delay locked loop control of claim 1 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a device deselect command.

4. The delay locked loop control of claim 1 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a predetermined number of no operation commands.

5. The delay locked loop control of claim 1 wherein the stabilization device is a delay device which indicates the device is stable after allowing passage of a predetermined interval from the time the command last received was received by the device.

6. The delay locked loop control of claim 1 wherein the stabilization device is a voltage detection device which indicates the device is stable by determining voltage fluctuations caused by receipt of the command last received have subsided.

7. The delay locked loop control of claim 1 wherein the delay lock also locks a delay locked loop clock device.

8. A delay locked loop control for a delay locked loop associated with a device responding to a system clock, the delay locked loop control comprising:

a device inactive decoder providing a device inactive signal when data will not be read from or written to the device; and

a delay lock coupled to the device inactive decoder for locking a stable delay interval on receiving the device inactive signal.

9. The delay locked loop control of claim 8 wherein the device inactive signal indicates data will not be read from or written to the device because the device has received a self-refresh command.

10. The delay locked loop control of claim 8 wherein the device inactive signal indicates data will not be read from or written to the device because the device has received a device deselect command.

11. The delay locked loop control of claim 8 wherein the device inactive signal indicates data will not be read from or written to the device because the device has received a predetermined number of no operation commands.

12. The delay locked loop control of claim 8 wherein the stable delay interval is reached after passage of a predetermined interval from the time the command last received was received by the device.

13. The delay locked loop control of claim 8 wherein the stable delay interval is reached when voltage fluctuations caused by receipt of the command last received have subsided.

14. The delay locked loop control of claim 8 wherein the delay lock also locks a delay locked loop clock device.

15. A DRAM device comprising:

a plurality of rows of DRAM memory cells, the DRAM memory cells receiving, storing, and outputting data;

an input/output system operably connected to the rows of DRAM memory cells for communicating data between the rows of DRAM memory cells and an external system;

a refresh system for refreshing contents of the DRAM memory cells;

a control logic array, the control logic array being operably interconnected with the input/output system and responsive to command from the external system; and

a delay locked loop subsystem synchronizing data communications between the input/output system and the external system, the delay locked loop having a delay locked loop control comprising:

a device inactive decoder providing a device inactive signal when the delay locked loop need not continue adjusting a delay interval to synchronize with the system clock;

a stabilization detection device providing a stabilization signal when the device is stable after reacting to a command applied to the device; and

a delay lock coupled to the device inactive decoder and the stabilization detection device for locking the delay interval on receiving both the device inactive signal and the stabilization detection signal.

16. The DRAM device of claim 15 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a self-refresh command.

17. The DRAM device of claim 15 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a device deselect command.

18. The DRAM device of claim 15 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a predetermined number of no operation commands.

19. The DRAM device of claim 15 wherein the stabilization device is a delay device which indicates the device has stabilized after passage of a predetermined interval from the time the command last received was received by the device.

20. The DRAM device of claim 15 wherein the stabilization device is a voltage detection device which indicates the device has stabilized by determining voltage fluctuations caused by receipt of the command last received have subsided.

21. The DRAM device of claim 15 wherein the delay lock also locks a delay locked loop clock device.

22. A computer system, comprising:

a processor;

an input device, operably connected to the processor, allowing data to be entered into the computer system;

an output device, operably connected to the processor, allowing data to be output from the computer system; and

a system memory operably connected to the processor through a system bus, the system memory comprising a plurality of DRAM devices having a plurality of rows of DRAM memory cells, the DRAM memory cells receiving, storing, and outputting data, at least one of the DRAM devices comprising:

an input/output system operably connecting the plurality of DRAM devices the computer system;

a refresh system for refreshing contents of the DRAM memory cells;

control logic, the control logic being operably interconnected with the input/output system and responsive to command from the external system;

a delay locked loop subsystem synchronizing data communications between the input/output system and the computer system; and

a delay locked loop control comprising:

a device inactive decoder providing a device inactive signal when the delay locked loop need not continue adjusting a delay interval to synchronize with the system clock;

a stabilization detection device providing a stabilization signal when the device is stable after reacting to a command applied to the device; and

a delay lock coupled to the device inactive decoder and the stabilization detection device for locking the delay interval on receiving both the device inactive signal and the stabilization detection signal.

23. The computer system of claim 22 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a self-refresh command.

24. The computer system of claim 22 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a device deselect command.

25. The computer system of claim 22 wherein the device inactive signal indicates the delay locked loop need not continue adjusting the delay interval because the device has received a predetermined number of no operation commands.

26. The computer system of claim 22 wherein the stabilization device is a delay device which indicates the device has stabilized after passage of a predetermined interval from the time the command last received was received by the device.

27. The computer system of claim 22 wherein the stabilization device is a voltage detection device which indicates the device has stabilized by determining voltage fluctuations caused by receipt of the command last received have subsided.

28. The computer system of claim 22 wherein the delay lock also locks a delay locked loop clock device.

29. A method for saving power in a delay locked loop associated with a device responding to a system clock, the method comprising:

determining when it is unnecessary for the delay locked loop to adjust a delay interval to synchronize with the system clock;

allowing the device to stabilize after receiving a command applied to the device before it was determined it is unnecessary for the delay locked loop to adjust the delay interval; and

locking the delay interval when it is unnecessary for the delay locked loop to adjust the delay interval and the device has stabilized.

30. The method of claim 29 wherein it is unnecessary for the delay locked loop to adjust the delay interval when the device is directed to a self-refresh state.

31. The method of claim 29 wherein it is unnecessary for the delay locked loop to adjust the delay interval when the device is deselected.

32. The method of claim 29 wherein it is unnecessary for the delay locked loop to adjust the delay interval when the device receives a predetermined number of no operation commands.

33. The method of claim 29 wherein the device is considered to have stabilized after passage of a predetermined interval from the time the command last received was received by the device.

34. The method of claim 29 wherein the device is considered to have stabilized once voltage fluctuations caused by receipt of the command last received have subsided.

35. The method of claim 29 further comprising locking a delay locked loop clock device.

36. A method for saving power in a delay locked loop associated with a device responding to a system clock, the method comprising:

determining when it is unnecessary for the delay locked loop to adjust a delay interval to synchronize with the system clock;

locking a stable delay interval when it is unnecessary for the delay locked loop to adjust the delay interval.

37. The method of claim 36 wherein it is unnecessary for the delay locked loop to adjust the delay interval when the device is directed to a self-refresh state.

38. The method of claim 36 wherein it is unnecessary for the delay locked loop to adjust the delay interval when the device is deselected.

39. The method of claim 36 wherein it is unnecessary for the delay locked loop to adjust the delay interval when the device receives a predetermined number of no operation commands.

40. The method of claim 36 wherein the device is considered to have stabilized after passage of a predetermined interval from the time the command last received was received by the device.

41. The method of claim 36 wherein the device is considered to have stabilized once voltage fluctuations caused by receipt of the command last received have subsided.

42. The method of claim 36 further comprising locking a delay locked loop clock device.